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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/938,106	08/23/2001	James M. Derderian	4832US (01-0104)	1038

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TRASK BRITT, P.C./ MICRON TECHNOLOGY
P.O. BOX 2550
SALT LAKE CITY, UT 84110

EXAMINER

IM, JUNGHWA M

ART UNIT	PAPER NUMBER
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2811

NOTIFICATION DATE	DELIVERY MODE
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01/17/2008

ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

USPTOMail@traskbritt.com

**Advisory Action
Before the Filing of an Appeal Brief**

Application No.

09/938,106

Applicant(s)

DERDERIAN, JAMES M.

Examiner

Junghwa M. Im

Art Unit

2811

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 21 December 2007 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:

- a) ☐ The period for reply expires _____ months from the mailing date of the final rejection.
b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
(a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
(b) ☐ They raise the issue of new matter (see NOTE below);
(c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
(d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).

4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☐ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
The status of the claim(s) is (or will be) as follows:
Claim(s) allowed: _____.
Claim(s) objected to: _____.
Claim(s) rejected: _____.
Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because:
See Continuation Sheet.
12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08) Paper No(s). _____.
13. ☐ Other: _____.



LYNNE GURLEY
SUPERVISORY PATENT EXAMINER
AV2811, TC2800

Continuation of 11. does NOT place the application in condition for allowance because:

Rejections under 35 U.S.C. § 112, First Paragraph and Second Paragraph are maintained.

Applicant's arguments are substantially identical in nature. And Applicant mainly argues that "... a second semiconductor device is entirely supported by discrete conductive elements that are located over portions of a first semiconductor device. FIG. 14 of the as-filed application illustrates an embodiment in which a semiconductor device 30b is entirely supported by intermediate conductive elements 38a that are located at least partially over another semiconductor device 30a. See also paragraphs [0015] and [0059]." Firstly, note that the claims recite the limitation "... second semiconductor ... being supported entire thereby ...," clearly implying that the second semiconductor device (the top semiconductor device) is entirely supported by the wires. Paragraphs [0015] and [0059] do not disclose this aspect at all. Rather, a next step in Fig. 15 explicitly shows that most part of the back surface of the second semiconductor device (the top semiconductor device) is supported by the adhesive, indicating the top semiconductor device is collectively supported by all the elements underneath it. Further, one of ordinary skill in the art understands that the weight of the top semiconductor device cannot be supported entirely by the wires. Therefore, Claims 23 and 45 fail to comply with the written description requirement. Additionally, it is confusing to understand how the entire weight of the semiconductor device can be supported entirely by the wires since there is no disclosure regarding this aspect.

Rejections under 35 U.S.C. § 102 is maintained.

Applicant argues that "... claims 23 and 45 that a second semiconductor device be 'entirely supported' by discrete conductive elements. It has been asserted that FIG. 4 of Wu shows wires 32 supporting the second semiconductor die 34. The description of Wu is limited to disposing wires 32 and glue over a lower semiconductor device 28 before positioning an upper semiconductor device 34 thereover. See, e.g., col. 3, lines 27-43." Note that claims 23 and 45 are rejected under 35 U.S.C. § 112, First Paragraph and Second Paragraph because of the reasons stated above. In particular, note that the instant invention does not disclose this aspect at all. Rather, as discussed above, Figures of the instant invention show that the second semiconductor die is supported by the adhesive and the wires. And Wu also shows that the second semiconductor die is supported by the adhesive (the glue) and the wires.